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2 CLAIMS

3 What is claimed is:

4 1. Structure comprising:

5 a printed circuit board containing a plurality of  
6 component contacts for receipt of electronic  
7 components;

8 a plurality of electrically conductive traces  
9 formed on said printed circuit board, each trace being  
10 electrically connected to a corresponding one of said  
11 component contacts; and

12 at least one integrated circuit mounted on a  
13 selected portion of said printed circuit board and  
14 containing a plurality of conductive leads, each of  
15 said conductive leads being electrically connected to a  
16 corresponding one of said electrically conductive  
17 traces formed on said printed circuit board thereby to  
18 form an electrically conductive path from each of said  
19 conductive contacts to the corresponding conductive  
20 leads on said at least one integrated circuit, said at  
21 least one integrated circuit being configurable by a  
22 user to interconnect selected electrically conductive  
23 traces on said printed circuit board to achieve a  
24 desired electrical function from the electronic  
25 components to be connected to said printed circuit  
26 board.

27 2. Structure as in Claim 1 wherein said printed  
28 circuit board contains more than one layer of conductive  
29 traces.  
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31 3. Structure as in Claim 1 wherein at least some of  
32 said plurality of electrical contacts comprise a plurality  
33 of holes in said printed circuit board, each hole being  
34 appropriate for receipt of a conductive lead of an  
35 electronic component.  
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37 4. Structure as in Claim 3 wherein the interior  
38 surface of each hole is plated with a conductive material.

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3 5. Structure as in Claim 4 wherein the conductive  
4 material on the interior of each hole is electrically  
5 connected to a corresponding one of said electrically  
6 conductive traces.

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8 6. Structure as in Claim 1 including a multiplicity  
9 of electronic components mounted on said printed circuit  
10 board, each electrical lead of said electronic components  
11 each making contact with a corresponding electrical contact  
12 selected from said plurality of electrical contacts.

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14 7. Structure as in Claim 6 wherein said at least one  
15 integrated circuit chip comprises one integrated circuit  
16 chip.

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18 8. Structure as in Claim 1 wherein at least some of  
19 said electrical contacts on said printed circuit board  
20 comprise pads, each pad being connected to a corresponding  
21 one of said plurality of electrically conductive traces  
22 formed on said printed circuit board.

23  
24 9. Structure as in Claim 8 wherein each pad is  
25 connected by a conductive lead to a hole formed through said  
26 printed circuit board, said hole being plated on its  
27 interior surface by a conductive material and said hole  
28 being in electrical contact with a corresponding one of said  
29 electrically conductive traces formed on said printed  
30 circuit board.

31  
32 10. Structure as in Claim 1 wherein said printed  
33 circuit board comprises:

34 a first portion thereof containing conductive  
35 traces for interconnecting electronic components formed  
36 thereon without the use of a programmable integrated  
37 circuit; and


38 a second portion thereof containing at least one  
programmable integrated circuit for interconnecting

1 electronic components formed on at least said second  
2 portion of said printed circuit board.  
3

4 11. A printed circuit board comprising:

5 a multiplicity of first electrical contacts formed  
6 in said printed circuit board for receipt of the leads  
7 of electronic components to be mounted on said printed  
8 circuit board;  
9

10 a corresponding multiplicity of second electrical  
11 contacts formed in a selected region of said printed  
12 circuit board for receipt of the leads on at least one  
13 package of at least one integrated circuit chip to be  
14 mounted on the printed circuit board for use in  
15 interconnecting selected ones of said multiplicity of  
16 first electrical contacts; and

17 conductive traces formed on said printed circuit  
18 board, each conductive trace uniquely interconnecting  
19 one first electrical contact to a corresponding second  
20 electrical contact.   
21

22 12. A printed circuit board as in Claim 11 including  
23 at least one integrated circuit mounted thereon wherein said  
24 at least one integrated circuit comprises a programmable  
25 circuit for interconnecting selected conductive traces  
26 formed on said printed circuit board thereby to form the  
27 electronic components to be contained thereon into a  
28 selected electrical circuit.

29 13. Structure as in Claim 12 including means for  
30 testing the state of said at least one programmable  
31 integrated circuit to determine the state of the signals on  
32 said conductive traces.  
33

34 14. Structure as in Claim 13 including means for  
35 transmitting control signals to said at least one integrated  
36 circuit for controlling the configuration of said at least  
37 one integrated circuit so as to control the interconnection  
38 of the conductive traces formed on said printed circuit

1 board.  
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3 15. Structure as in Claim 14 including at least one  
4 programmable integrated circuit mounted on said printed  
5 circuit board for interconnecting selected traces formed on  
6 said printed circuit board.  
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8 16. Structure as in Claim 15 wherein said printed  
9 circuit board comprises:

10 a first portion thereof containing conductive  
11 traces for interconnecting electronic components formed  
12 thereon without the use of a programmable integrated  
13 circuit; and

14 a second portion thereof containing at least one  
15 programmable integrated circuit for interconnecting  
16 electronic components formed on at least said second  
17 portion of said printed circuit board.  
18

19 17. A printed circuit board comprising:  
20

21 a multiplicity of component holes for receipt of  
22 leads of electronic components;

23 a corresponding multiplicity of PIC holes for  
24 receipt of the leads on the package or packages of a  
25 programmable interconnect chip or chips; and

26 one or more layers of conductive traces formed on  
27 said printed circuit board, each conductive trace  
28 uniquely connecting one component hole to one PIC hole.  
29

30 18. Structure as in Claim 17 wherein said printed  
31 circuit board comprises:

32 a first portion thereof containing conductive  
33 traces for interconnecting electronic components formed  
34 thereon without the use of a programmable integrated  
35 circuit; and

36 a second portion thereof containing at least one  
37 programmable integrated circuit for interconnecting  
38 electronic components formed on at least said second  
portion of said printed circuit board.

19. The method of configuring an electronic system on a printed circuit board comprising the steps of:

- creating a computer model of the programmable PC board containing a plurality of component contacts for receipt of the leads of electronic components to be mounted on said printed circuit board, a corresponding plurality of PIC contacts for receipt of the leads of one or more programmable interconnect chips ("PIC") for use in interconnecting selected electronic components and conductive traces, each conductive trace connecting one component contact to one PIC contact;
- simulating the placement and routing of select electronic components on the component contacts;
- simulating the electrical performance of the system with the electrical components interconnected by the PIC;
- interconnecting the electronic components in a desired fashion by configuring the PIC to achieve such interconnection;
- determining the system performance and system characteristics with the electronic components so interconnected by simulating and/or testing the system so interconnected; and
- repeating the above steps making those changes in placement of electronic components as indicated to be required by the simulation or test results until the above steps yield an electronic system which yields the desired characteristics and functional performance.

20. A programmable interconnect chip for use in interconnecting electronic components formed on a printed circuit board, said chip comprising:

- a first set of conductive leads formed in a first direction across the surface of said chip, each of said conductive leads comprising one or more conductive segments, portions of selected ones of said segments being connected to pads on the surface of said

1 programmable interconnect chip, each of said pads being  
2 adapted for contact to a corresponding contact on the  
3 printed circuit board;

4 a second set of conductors formed on said  
5 programmable interconnect chip in a second direction  
6 not parallel to said first direction, each conductive  
7 lead in said second set of conductive leads comprising  
8 one or more segments; and

9 means for electrically interconnecting selected  
10 ones of said conductive leads in said first set of  
11 conductive leads to one or more of said conductive  
12 leads in said second set of conductive leads.

13 21. Structure as in Claim 20 wherein said programmable  
14 interconnect chip comprises:

15 active transistor in said programmable  
16 interconnect chip;

17 means for electrically connecting selected ones of  
18 the segments of conductive leads in said first set of  
19 conductive leads and in said second set of conductive  
20 leads to programmable transistors in the substrate of  
21 said programmable interconnect chip; and

22 means for programming said programmable  
23 transistors in said interconnect chip so as to turn on  
24 selected ones of the transistors in said programmable  
25 interconnect chip to form desired interconnections  
26 between selected contacts on said printed circuit  
27 board.

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29 *Sub E2* 22. Structure as in Claim 20 wherein said means for  
30 electrically interconnecting comprise a plurality of  
31 interconnect structures, each interconnect structure  
32 comprising:

33 a first conductive layer comprising a portion of  
34 the conductive segment of a conductive lead in said  
35 first set of leads;

36 a second conductive layer comprising a portion of  
37 the conductive segment of a conductive lead in said  
38

1 second set of conductive leads; and  
2 dielectric formed between said first conductive  
3 lead and said second conductive lead, said dielectric  
4 being capable of being made conductive by the  
5 application of a selected voltage thereto, thereby to  
6 form an electrically conductive path from said  
7 conductive segment in said first set of conductive  
8 leads to said conductive segment in said second set of  
9 conductive leads.

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